AMENDMENTS TO THE SPECIFICATION

Please add the following paragraph at the beginning of the Specification:

CROSS-REFERENCE TO RELATED APPLICATIONS

[0000] This application claims the benefit of U.S. Provisional Application No. 60/452,143, filed on March 4, 2003.

Please replace paragraph [0059] with the following amended paragraph:

[0059] One or more logic blocks, including sub-blocks, from IC design 101 is obtained at 351 for configuring a test case design from 343. Notably, IC design 101 may be described using Verilog, and thus may include one or more "tranif" Verilog statements for reasons described below in additional detail (further details on the "tranif" Verilog statements are found in the chapter on bidirectional pass switches using "tranif0 and "tranif1" keywords in the Verilog Language Reference Manual (LRM) ~~found at http://www.ee.eng.hawaii.edu/~msmith/ASICs/HTML/Verilog/Verilog.htm,~~ Chapter 7.6~~, which is herein incorporated by reference~~). At 351, a logic block is level abstracted including application of memory states 348. Notably, at 351 application of memory states 348 may be done prior to level abstraction or after level abstraction, for example using a logic synthesis tool such as Design Compiler from Synopsys, or by a logic level abstraction tool. However, for clarity, it will be assumed that at 351 level abstraction is used to apply memory states 348 though such application of memory states may be done independently from level abstraction.

8/4/06